PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

PCT

To: MICHAEL J. MALLIE
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BLVD. 7TH FLOOR
LOS ANGELES, CA 90025

WRITTEN OPINION
(PCT Rule 66)

Date of Mailing *(day/month/year)*

Applicant's or agent's file reference P11706PCT	REPLY DUE within TWO months from the above date of mailing

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US02/16557	23 MAY 2002	29 MAY 2001

International Patent Classification (IPC) or both national classification and IPC
IPC(7):G06K 9/36 and US Cl.: 382/240

Applicant
INTEL CORPORATION

1. This written opinion is the first (first, etc.) drawn by this International Preliminary Examining Authority.

2. This opinion contains indications relating to the following items:

- I [X] Basis of the opinion
- II [ ] Priority
- III [ ] Non-establishment of opinion with regard to novelty, inventive step or industrial applicability
- IV [ ] Lack of unity of invention
- V [X] Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI [ ] Certain documents cited
- VII [ ] Certain defects in the international application
- VIII [ ] Certain observations on the international application

3. The applicant is hereby invited to reply to this opinion.

When? See the time limit indicated above. ~~The applicant may, before the expiration of that time limit, request this Authority to grant an extension., see Rule 66.2(d).~~

How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.

Also For an additional opportunity to submit amendments, see Rule 66.4.
For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4 *bis*.
For an informal communication with the examiner, see Rule 66.6.

If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary examination report must be established according to Rule 69.2 is: 29 SEPTEMBER 2003

Name and mailing address of the IPEA/US	Authorized officer
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Date of Mailing *(day/month/year)*	27 AUG 2003
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International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
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International Patent Classification (IPC) or both national classification and IPC
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Applicant
INTEL CORPORATION

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Form PCT/IPEA/408 (cover sheet) (July 1998)*

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

TIME LIMIT:

The time limit set for response to a Written Opinion may not be extended. 37 CFR 1.484(d). Any response received after the expiration of the time limit set in the Written Opinion will not be considered in preparing the International Preliminary Examination Report.

V. 2. REASONED STATEMENTS - CITATIONS AND EXPLANATIONS (Continued):

or more conditions applied to the coefficient being coded is true of false (refer for example to column 6, lines 16-49).

With regard to claim 10, Shapiro describes wherein at least one of the one or more conditions that the architecture is adapted to apply relates to the magnitude of the coefficient being coded relative to a threshold (refer for example to column 6, lines 16-26).

As to claim 11, Shapiro describes wherein the threshold of the next successive pass from a particular pass is a multiplicative factor greater than one times the threshold of the particular pass (refer for example to column 1, line 35 through column 9, line 26).

With regard to claim 12, Shapiro describes wherein the multiplicative factor is two (refer for example to column 8, lines 50-55 and to column 9, lines 9-10).

In regard to claim 13, Shapiro describes applying a bit-based conditional decoding to the encoded DWT coefficients (refer for example to column 21, lines 22-54).

With regard to claim 14, Shapiro describes wherein applying a bit-based conditional decoding comprises decoding using one or more binary-valued variables, the value depending on whether one or more conditions was true of false when applied during encoding to the coefficient being decoded (refer for example to column 22, lines 22-34).

As to claim 15, Shapiro describes wherein at least one of the one or more conditions relates to the magnitude relative to a threshold, during encoding, of the coefficient being decoded (refer for example to column 22, lines 22-34).

In regard to claim 16, Shapiro describes wherein applying a bit-based conditional decoding comprises applying a bit-based conditional decoding to encoded DWT coefficients having relatively low energy (refer for example to column 1, line 53 through column 2, line13 and to column 4, lines 8-11).

With regard to claim 17, Shapiro describes an architecture to apply a bit-based conditional embedded zero tree coding to the discrete wavelet transform (DWT) coefficients that have been encoded (see figure 18 and refer for example to column 24, lines 22-68).

As to claim 18, Shapiro describes wherein the hardware comprises at least one of the following: hardware, software, firmware, and any combination thereof (as clearly illustrated in figure 18).

In regard to claim 19, Shapiro describes wherein the architecture is adapted to apply a bit-based conditional decoding using one or more binary-valued variables, the value depending on whether one or more conditions applied to the coefficient being decoded was true of false when applied during the encoding to the coefficient being decoded (refer for example to column 22, lines 22-34).

With regard to claim 20, Shapiro describes wherein at least one of the one or more conditions relates to the magnitude relative to a threshold, during encoding, of the coefficient being decoded (refer for example to column 22, lines 22-34).

As to claim 21, Shapiro describes applying a bit-based conditional coding to the DWT coefficients (refer for example to column 5, lines 49-53).

With regard to claim 22, Shapiro describes wherein the instructions, when executed, further result in applying a bit-based conditional coding comprises coding using one or more binary-valued variables, the value depending on whether one or more conditions applied to the coefficient being coded is true of false (refer for example to column 6, lines 16-26).

In regard to claim 23, Shapiro describes wherein the instructions, when executed, further result in at least one of the one or more conditions relates to the magnitude of the coefficient being coded relative to a threshold (refer for example to column 6, lines 16-26).

With regard to claim 24, Shapiro describes applying a bit-based conditional decoding to the DWT coefficients (refer for example to column 21, lines 22-54).

As to claim 25, Shapiro describes wherein the instructions, when executed, further result in applying a bit-based conditional decoding comprises decoding using one or more binary-valued variables, the value depending on whether one or more conditions was true of false when applied during encoding of the coefficient being decoded (refer for example to column 22, lines 22-34).

In regard to claim 26, Shapiro describes wherein the instructions, when executed, further result in at least one of the one or more conditions relating to the magnitude relative to a threshold, during encoding, of the coefficient being decoded (refer for example to column 22, lines 22-34).

With regard to claim 27, Shapiro describes a computing platform (see figure 14); the computing platform including a processor, a memory, and a bus for communication to occur between the processor and memory (as clearly illustrated in figure 14, element 1418 is a microprocessor as stated in column 21, lines 7-10); the computer platform including an

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

architecture adapted to, during operation, perform a method of embedded zero tree coding discrete wavelet transform (DWT) coefficients by applying a bit-based conditional coding to the DWT coefficients (refer for example to column 5, lines 49-53).
As to claim 28, Shapiro describes wherein the hardware comprises at least one of the following: hardware, software, firmware, and any combination thereof (as clearly illustrated in figure 14).
In regard to claim 29, Shapiro describes wherein the architecture is adapted to, during operation, apply a bit-based conditional coding using one or more binary-valued variables, the value depending on whether one or more conditions applied to the coefficient being coded is true of false (refer for example to column 6, lines 16-26).
With regard to claim 30, Shapiro describes a computing platform (see figure 18); the computing platform including a processor, a memory, and a bus for communication to occur between the processor and memory (as clearly illustrated in figure 18, element 1836 is a processor as discussed in column 24, line 66); the computer platform including an architecture adapted to, during operation, perform a method of embedded zero tree decoding encoded discrete wavelet transform (DWT) coefficients by applying a bit-based conditional decoding to the DWT coefficients (refer for example to column 24, lines 22-68).
As to claim 31, Shapiro describes wherein the hardware comprises at least one of the following: hardware, software, firmware, and any combination thereof (as clearly illustrated in figure 18).
In regard to claim 32, Shapiro describes wherein the architecture is adapted to, during operation, apply a bit-based conditional decoding using one or more binary-valued variables, the value depending on whether one or more conditions applied to the coefficient being decoded was true of false when applied during the encoding to the coefficient being decoded (refer for example to column 22, lines 22-34).

---------- NEW CITATIONS ----------

US 5,321,776 A (SHAPIRO) 14 JUNE 1994, see figures 14 and 18, column 3, line 50 through column 6, line 68, and column 20, line 34 through column 24, line 68.

US 6,157,746 A (SODAGAR et al.) 05 DECEMBER 2000, see figures 1-2, column 4, line 41 through column 5, line 19, and column 9, line 35 through column 10, line 13.

US 6,359,928 B1 (WANG et al.) 19 MARCH 2002, see figure 5, and column 5, line 36 through column 6, line 49.